Analog Reinvented

ES9023

SABRE **Premier Stereo DAC with 2Vrms Driver**

Datasheet

Device	Description	DNR (dB)	Power Supply (Output Level)	No DC-blocking capacitor	Pop-Noise Free	Package
FS9023	Sabre Premier Stereo DAC with 2Vrms Op-Amp Driver	112	+3.6V (2Vrms) +3.3V (1.9Vrms)	√	√	16-SOP

The ES9023 is a 24-bit stereo audio DAC with an integrated 2Vrms op-amp driver. Powered by the industry proven Sabre DAC technology, the ES9023 combines best-sounding audio with lowest system cost and highest performance into the ideal D/A converter for line-level output applications such as Blu-ray players, CD/DVD players, set-top boxes, digital TVs and audio receivers.

With patented Hyperstream™ architecture and Time Domain Jitter Eliminator, the ES9023 delivers jitter-free studio quality audio with 112dB DNR.

Using an integrated charge pump to generate the negative supply, the ES9023 can operate from a single AVCC supply to drive a ground-referenced 2Vrms output, eliminating the need for output dc-blocking capacitors. Optionally, the output level can be adjusted by using an external resistor, allowing for output level below 2Vrms. Pop-noise is eliminated through a comprehensive suppression on power up/down, mute, reset, loss of power or clock. Dedicated control/status pins allow easy system integration without the need for microcontroller programming.

FEATURE	BENEFIT
Sabre DAC and 2Vrms op-amp driver integration	▪ Lowest system cost by minimizing external components ▪ Highest performance ▪ Best sounding audio – powered by Sabre DAC technology
Patented HyperStream™ and Jitter Elimination Architecture	▪ Best dynamic range: 112dB ▪ Jitter Immune
Adjustable output level	▪ Allow designer to customize output level (up to 2Vrms) based on application requirements via an external resistor
Ground reference output	▪ Reduce cost by eliminating blocking capacitors
Pop-noise suppression	▪ Pop-free on power up/down, mute and reset
Dedicated control/status pins ▪ I2S or left-justified select ▪ Soft mute enable ▪ Zero detect output	▪ Easy to use – no programming required
Charge pump for negative supply	▪ Single AVCC simplifies power supply
Low power consumption in 16-SOP	▪ Simply power supply and reduce PCB size

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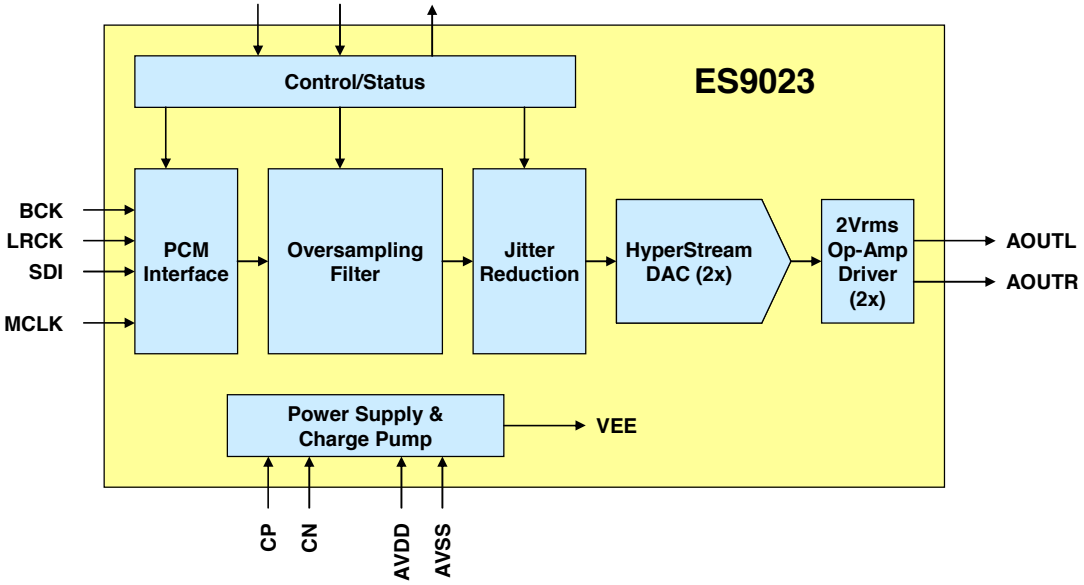
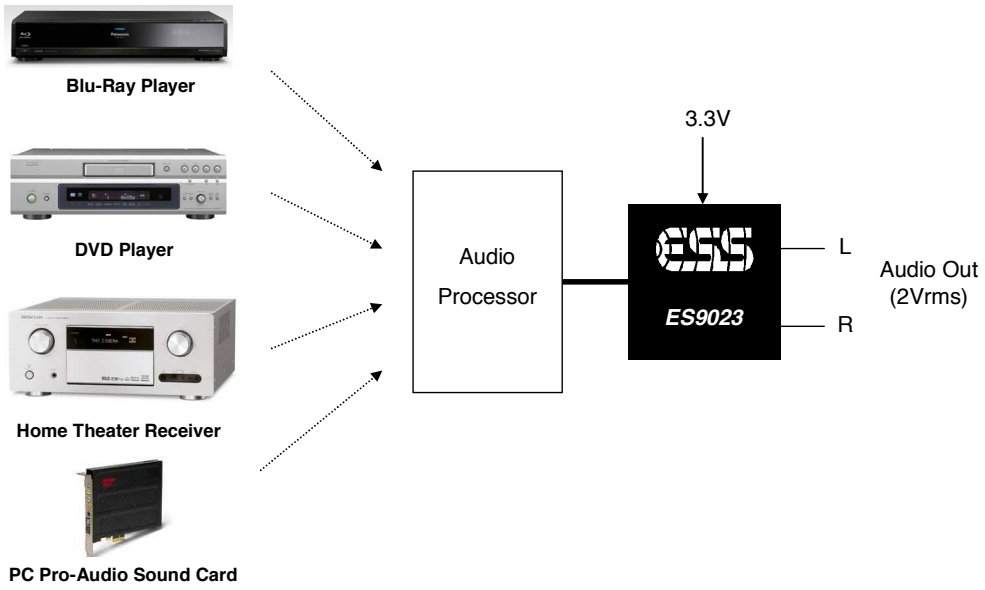
FUNCTIONAL BLOCK DIAGRAM

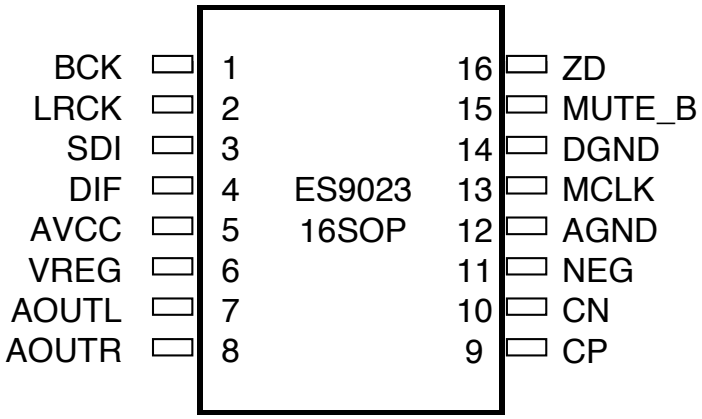


APPLICATION DIAGRAM



ES9023 Datasheet

PIN LAYOUT



PIN DESCRIPTION

Pin #	Name	Type	Pin Description
1	BCK	I	I2S Bit Clock
2	LRCK	I	I2S L/R (Word) Clock
3	SDI	I	I2S Serial Data Input
4	DIF	I	Input to select Left Justified or I2S data
5	AVCC	P	AVCC Power supply
6	VREG	P	Analog Reference Output
7	AOUTL	O	Left Analog Output
8	AOUTR	O	Right Analog Output
9	CP	I	Positive Terminal of External Charge Pump Capacitor
10	CN	I	Negative Terminal of External Charge Pump Capacitor
11	NEG	P	Negative Supply (Internally Generated)
12	AGND	P	Analog Ground
13	MCLK	I	Master (System) Clock
14	DGND	P	Ground
15	MUTE_B	I	Active Low Mute Input
16	ZD	O	Zero Detect Output

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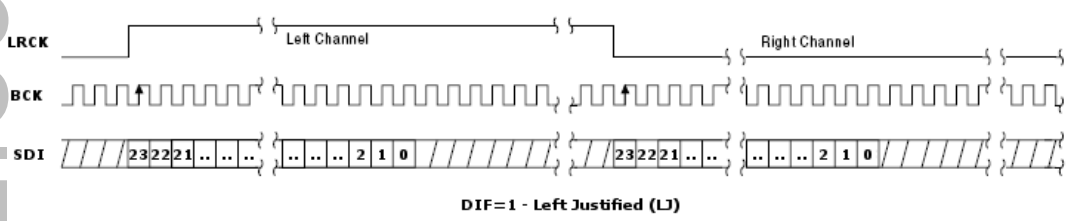
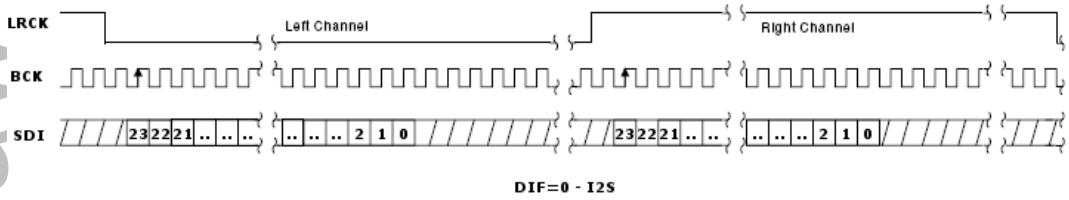
FUNCTIONAL DESCRIPTION

I2S Decoder:
Run by the I2S bit clock, typically a 64FS clock, the I2S Decoder translates the incoming I2S data to 24-bit signed PCM data. If a smaller bit-width is used, the remaining is 'zero-padded'. Driving the DIF pin low will set the DAC in I2S mode while driving the pin high will set the DAC in LJ mode. Below is a timing diagram illustrating the two modes (LJ and I2S) utilized by the ES9023.





Zero Detect:
The zero-detect function outputs an external status signal (ZD) based on a zero-valued input for a given number of clock cycles. The ZD output signal is set high when both data channels are zero for 8192 LRCK cycles.

MCLK
Asynchronous mode: MCLK must be > 192*fs.
Synchronous mode: Please see table below for supported configurations.

LRCK (kHz)	MCLK (MHz)						
fs	128fs	192fs	256fs	384fs	512fs	768fs	1152fs
32	-	-	-	12.288	16.384	24.576	36.864
44.1	-	-	11.2896	16.9344	22.5792	33.8688	-
48	-	-	12.288	18.432	24.576	36.864	-
88.2	11.2896	16.9344	22.5792	33.8688	45.1584	-	-
96	12.288	18.432	24.576	36.864	49.152	-	-
176.4	22.5792	33.8688	45.1584	-	-	-	-
192	24.576	36.864	49.152	-	-	-	-

For best performance. 256fs or greater is recommended for 32kHz to 96kHz sampling.

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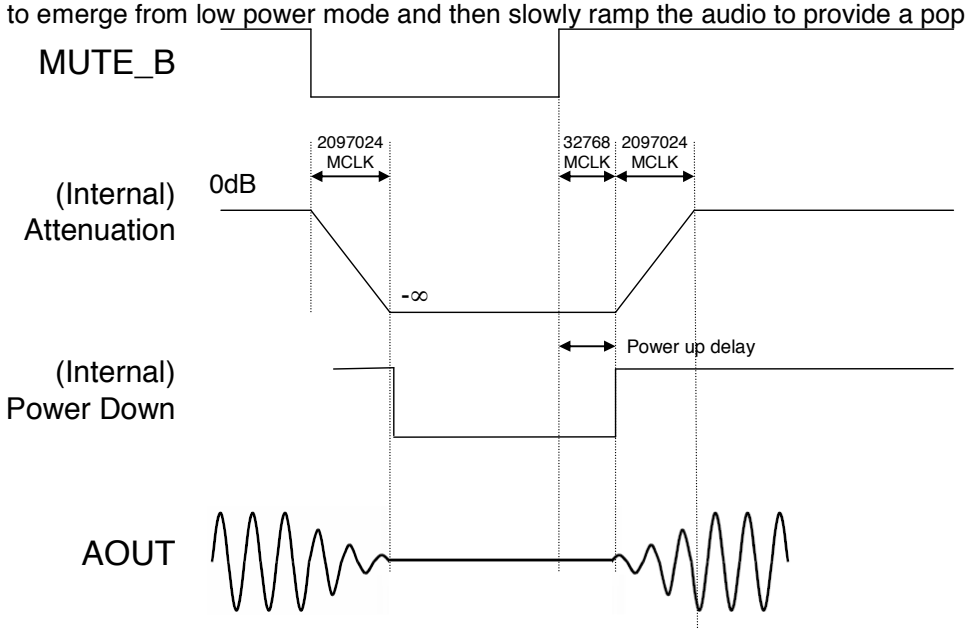
MUTE_B Pin (Active Low)

This input pin provides the ability to slowly ramp down the audio volume, and then enter low power standby. Release of mute will cause the ES9023 to emerge from low power mode and then slowly ramp the audio to provide a pop free startup.

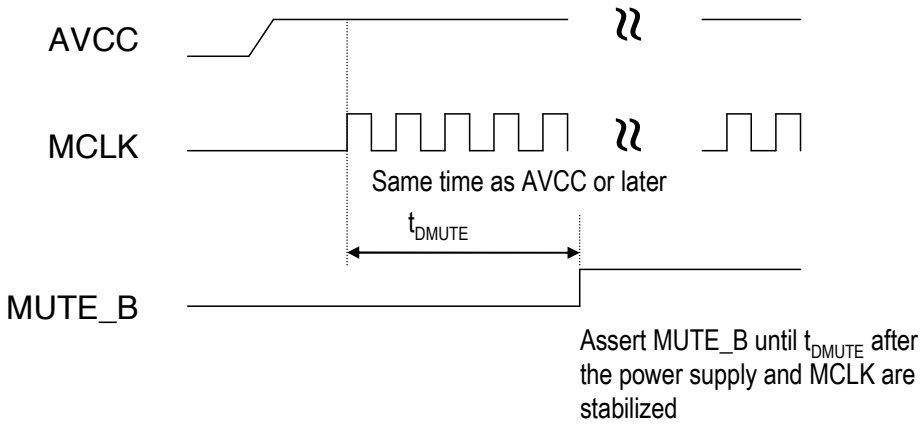


Activation/release of the MUTE_B input pin initiates a sequence of internal events detailed below:

- On assertion of the MUTE_B pin
  - The output signal will ramp to the -∞ level. The ramping takes 2097024 MCLK cycles.
  - After the output signal reaches the -∞ level, analog section is turned off and the ES9023 enters a low power standby state.
- On release of the MUTE_B pin:
  - The ES9023 emerges from low power standby, starts an internal counter and activates the analog section
  - During the delay counter time, the internal charge pump and Vref stabilize.
  - When the counter reaches 32768 MCLK cycles, the audio signal is applied and the volume is ramped over 2097024 MCLK cycles to maximum.

To minimize pop noise at power up, an external circuit should be used to hold the MUTE_B pin asserted until t_{DMUTE} (see p[illegible]) after the power supply and MCLK are stabilized.

- This can be realized using a reset IC, an MCU GPIO pin (default to low at power-up and changed to high by software later), or an RC time delay on this pin.
- If MUTE_B pin is released too early, pop noise may occur due to the ramp-up of internal voltage.



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DAC/OP-AMP:
Each Hyperstream DAC is followed by an op-amp circuit for each channel. A pop suppression circuit is added on the output to eliminate any “pop” noise that may be heard during muting, un-muting, power-up and power-down sequences. In some conditions, pop noise may be audible. See the MUTE_B pin section above.

Charge Pump (Negative Voltage Generation):
This is an analog circuit required to generate an internal negative supply. With positive and negative supplies, the op-amp circuits will be able to generate a ground-referenced 2Vrms output.

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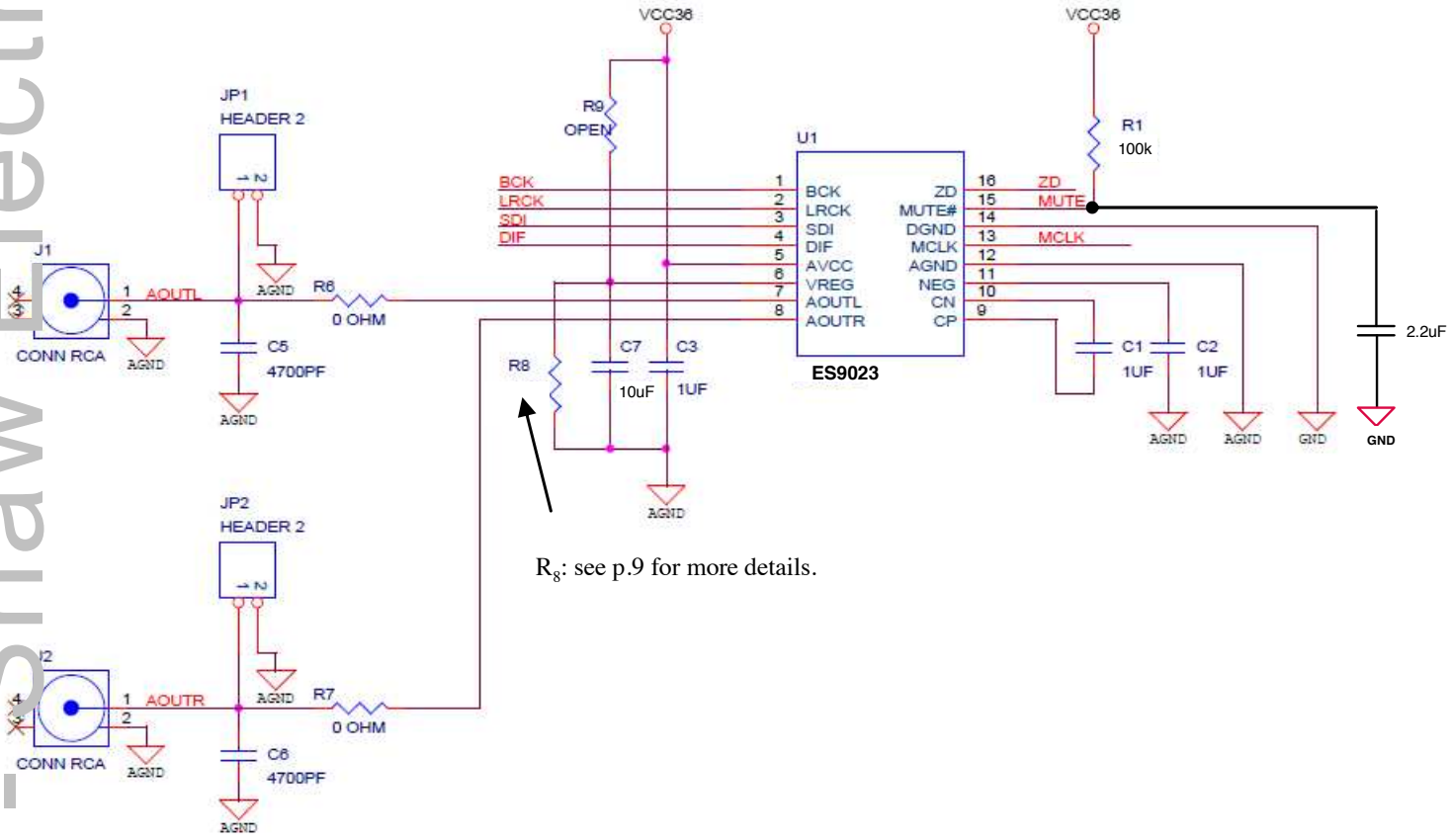
APPLICATION DIAGRAM



R_8: see p.9 for more details.

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ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PAREMETER	RATING
Storage temperature	-65°C to 105°C
Voltage range for 5V tolerant pins	-0.5V to +5.5V
Voltage range for all other pins	-0.5V to (AVCC+0.5V)

WARNING: Stress beyond those listed under the Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the Recommended Operating Conditions section of this specification is not implied. Exposure to the Absolute Maximum Ratings conditions for extended periods may affect device reliability.

WARNING: Electrostatic Discharge (ESD) can damage this device. Proper procedures must be followed to avoid ESD when handling this device.

RECOMMENDED OPERATING CONDITIONS

PAREMETER	SYMBOL	CONDITIONS
Operating temperature	TA	0℃ to 70℃
Power supply voltage	AVCC	3.6V ± 5%, 31 mA nominal (*1), or 3.3V ± 5%, 23 mA nominal (*1)

Note

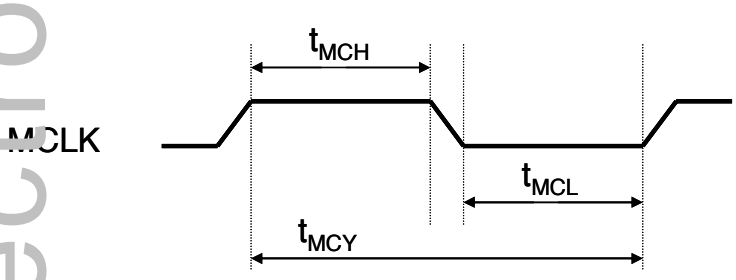
(*1) fs =48kHz, MCLK=27MHz, I2S input, output unloaded

DC ELECTRICAL CHARACTERISTICS

Table 1 DC Electrical Characteristics

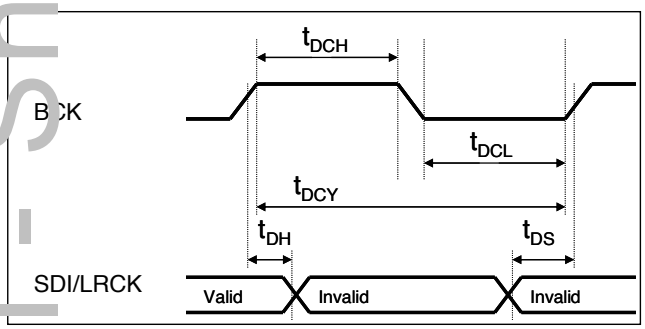
SYMBOL	PARAMETER	MIN	MAX	UNIT	COMMENTS
V_{IH}	High-level input voltage	2	AVCC	V	All inputs TTL levels except CLK and 5V tolerant input pins
		2	5.5	V	All 5V tolerant inputs
V_{IL}	Low-level input voltage	-0.3	0.8	V	All input TTL levels except CLK
V_{CLKH}	CLK high-level input	2	AVCC+0.25	V	TTL level input
V_{CLKL}	CLK low-level input	-0.3	0.8	V	
V_{OH}	High-level output voltage	3		V	I_{OH} = 1mA
V_{OL}	Low-level-output voltage		0.45	V	I_{OL} = 4mA
I_{IL}	Input leakage current		±15	µA	
I_{OZ}	Output leakage current		±15		
C_{IN}	Input capacitance		10	pF	fc = 1MHz
C_{IO}	Input/output capacitance		12		
C_{CLK}	CLK capacitance		20	pF	fc = 1MHz

MCLK Timing



Parameter	Symbol	Min	Max	Unit
MCLK pulse width high	T_{MCH}	9		ns
MCLK pulse width low	T_{MCL}	9		ns
MCLK cycle time	T_{MCY}	20		ns
MCLK duty cycle		45:55	55:45	

Audio Interface Timing



Parameter	Symbol	Min	Max	Unit
BCK pulse width high	t_{DCH}	20		ns
BCK pulse width low	t_{DCL}	20		ns
BCK cycle time	t_{DCY}	44		ns
BCK duty cycle		45:55	55:45	
SDI/LRCK set-up time to BCK rising edge	t_{DS}	2		ns
SDI/LRCK hold time to BCK rising edge	t_{DH}	2		ns

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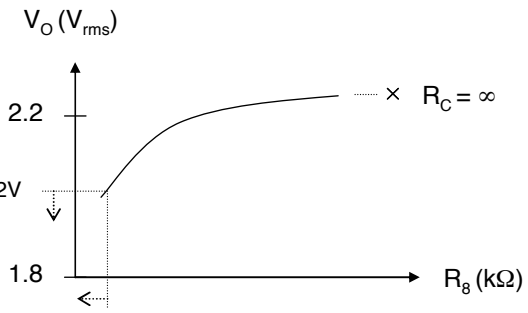
ANALOG PERFORMANCE

Test Conditions (unless otherwise stated)

1. T_A=25°C, AVCC=3.6V, fs =44.1kHz, MCLK=27Mhz, 24-bit data, R_L≥10kΩ, Signal Frequency=1kHz
2. SNR/DNR: A-weighted over 20-22kHz in averaging mode
3. THD+N: un-weighted over 20-22kHz bandwidth

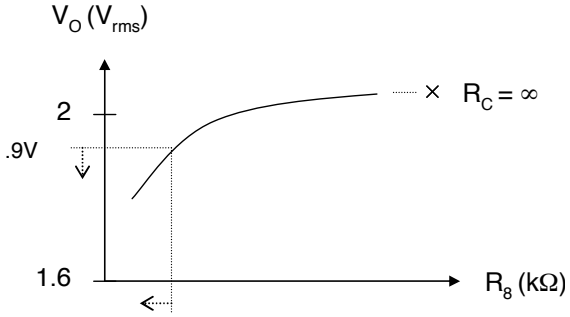
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
PCM sampling rate	f_S				200	kHz
Mute Delay	t_{DMUTE}		500			mS
DYNAMIC PERFORMANCE						
DNR (A-weighted)		-60dBFS		112		dB-A
THD+N		0dBFS		0.002	0.006	%
		-3dBFS			0.005	%
Interchannel Isolation				100		dB
DC Accuracy						
Absolute DC Offset				<4		mV
Output Voltage	V_O	0dBFS, AVCC=3.6V, R_8=130kΩ		2.0		Vrms
		0dBFS, AVCC=3.3V, R_8=220kΩ		1.9		Vrms
Load Resistance	R_L		5			kΩ
Digital Filter Performance						
Pass band		±0.005dB			0.454	fs
		-3dB			0.49	fs
Stop band		< -115dB	0.546			dB
Group Delay				35/fs		S

AVCC=3.6V



Select R_8 ≤130kΩ for no clipping

AVCC=3.3V



Select R_8 ≤ 220kΩ for no clipping

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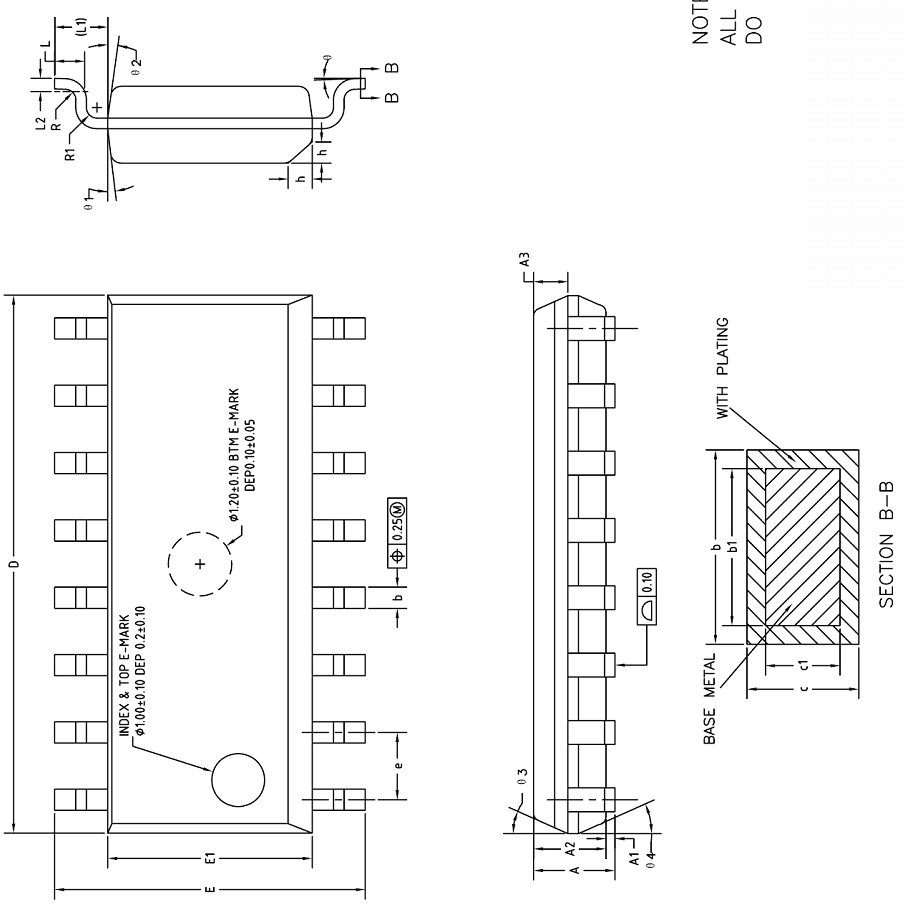
16 Pin SOP Mechanical Dimensions

COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	1.35	1.60	1.75
A1	0.10	0.15	0.25
A2	1.25	1.45	1.65
A3	0.55	0.65	0.75
b	0.36	–	0.51
b1	0.35	0.40	0.45
c	0.17	–	0.25
c1	0.17	0.20	0.23
D	9.86	9.96	10.06
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27BSC	
L	0.45	0.60	0.80
L1		1.04REF	
L2		0.25BSC	
R	0.07	–	–
R1	0.07	–	–
h	0.30	0.40	0.50
θ	0°	–	8°
θ 1	6°	8°	10°
θ 2	6°	8°	10°
θ 3	5°	7°	9°
θ 4	5°	7°	9°

NOTES:
ALL DIMENSIONS MEET JEDEC STANDARD MS-012 AC
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.



The solder paste and PCB finish/plating must be 100% lead-free in order to ensure proper solderability.

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Reflow Process Considerations

For lead-free soldering, the characterization and optimization of the reflow process is the most important factor you need to consider.

The lead-free alloy solder has a melting point of 217℃. This alloy requires a minimum reflow temperat ure of 235℃ to ensure good wetting. The maximum reflow temperature is in the 245℃ to 260℃ range, depending on the package size *(Table RPC-2)*. This narrows the process window for lead-free soldering to 10℃ to 20℃.

The increase in peak reflow temperature in combination with the narrow process window makes the development of an optimal reflow profile a critical factor for ensuring a successful lead-free assembly process. The major factors contributing to the development of an optimal thermal profile are the size and weight of the assembly, the density of the components, the mix of large and small components, and

the paste chemistry being used.

Reflow profiling needs to be performed by attaching calibrated thermocouples well adhered to the device as well as other critical locations on the board to ensure that all components are heated to temperatures above the minimum reflow temperatures and that smaller components do not exceed the maximum temperature limits *(Table RPC-2)*.

To ensure that all packages can be successfully and reliably assembled, the reflow profiles studied and recommended by ESS are based on the JEDEC/IPC standard J-STD-020 revision D.1.

Figure RPC-1. IR/Convection Reflow Profile (IPC/JEDEC J-STD-020D.1)

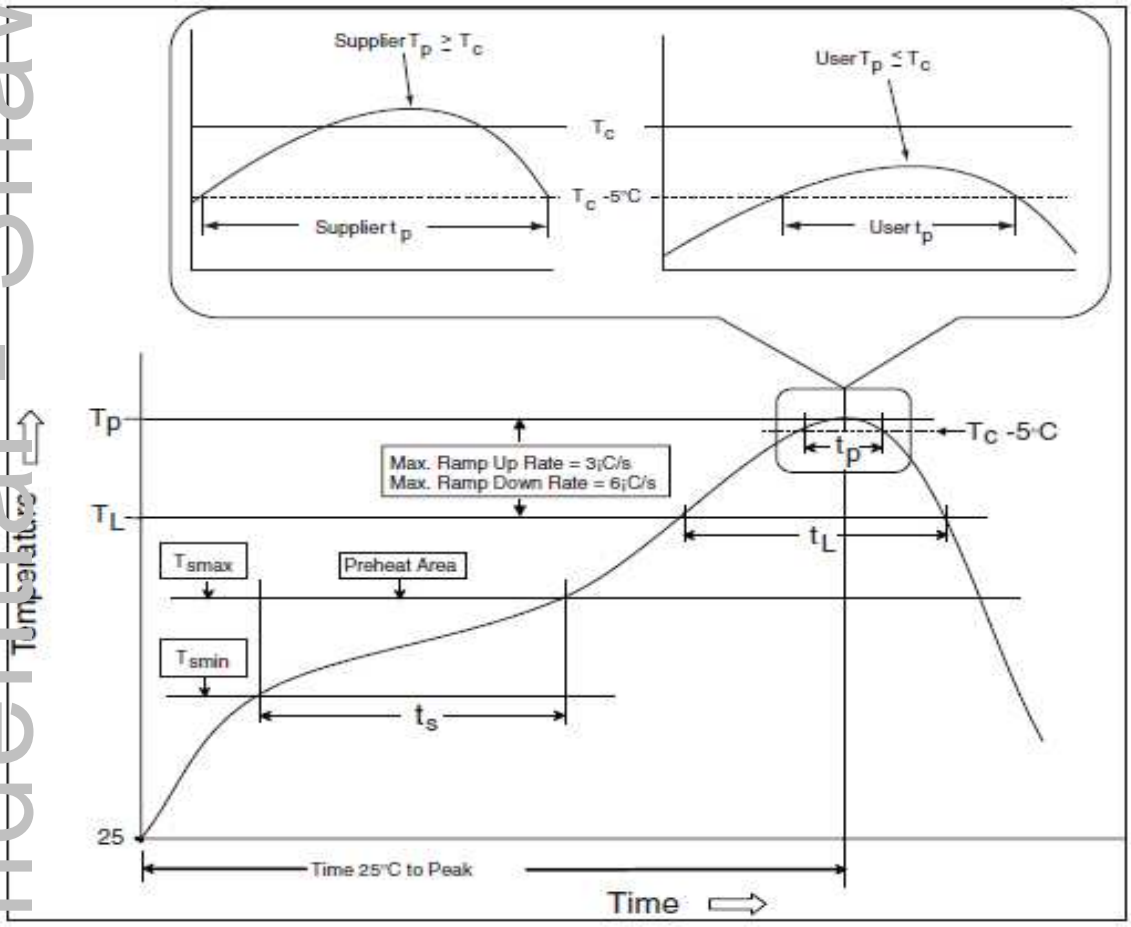

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Table RPC-1 Classification reflow profile

Profile Feature	Pb-Free Assembly
Preheat/Soak Temperature Min (Tsmin) Temperature Max (Tsmax) Time (ts) from (Tsmin to Tsmax)	 150 ℃ 200 ℃ 60-120 seconds
Ramp-up rate (TL to Tp)	3 ℃/second max.
Liquidous temperature (TL) Time (tL) maintained above TL	217 ℃ 60-150 seconds
Peak package body temperature (Tp)	For users Tp must not exceed the classification temp in Table RPC-2. For suppliers Tp must equal or exceed the Classification temp in Table RPC-2.
Time (tp)* within 5 ℃ of the specified classification temperature (Tc), see Figure RPC-1	30* seconds
Ramp-down rate (Tp to TL)	℃/second max.
Time 25 ℃ to peak temperature	8 minutes max.
* Tolerance for peak profile temperature (Tp) is defined as a supplier minimum and a user maximum.	

Note 1: All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e., dead-bug), Tp **shall** be within ± 2 ℃ of the live-bug Tp and still meet the Tc requirements, otherwise, the profile **shall** be adjusted to achieve the latter. To accurately measure actual peak package body temperatures refer to JEP140 for recommended thermocouple use.

Note 2: Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table RPC-1.
For example, if Tc is 260 ℃ and time tp is 30 seco nds, this means the following for the supplier and the user.
For a supplier: The peak temperature must be at least 260 ℃. The time above 255 ℃ must be at least 3 0 seconds.
For a user: The peak temperature must not exceed 260 ℃. The time above 255 ℃ must not exceed 30 seco nds.

Note 3: All components in the test load **shall** meet the classification profile requirements.

Table RPC-2 Pb-Free Process - Classification Temperatures (Tc)

Package Thickness	Volume mm3<350	Volume mm3 350 - 2000	Volume mm3 >2000
<1.6 mm	260 ℃	260 ℃	260 ℃
1.6 mm - 2.5 mm	260 ℃	250 ℃	245 ℃
>2.5 mm	250 ℃	245 ℃	245 ℃

Note 1: At the discretion of the device manufacturer, but not the board assembler/user, the maximum peak package body temperature (Tp) can exceed the values specified in Table RPC-2. The use of a higher Tp does not change the classification temperature (Tc).

Note 2: Package volume excludes external terminals (e.g., balls, bumps, lands, leads) and/or nonintegral heat sinks.

Note 3: The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.

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ORDERING INFORMATION

Part Number	Description	Package
ES9023P	Sabre Premier Stereo DAC with 2Vrms Driver	16-SOP

The letter P at the end of the part number identifies the package type SOP.

REVISION HISTORY

Revision	Date	Notes
0.1	September 17, 2010	Initial version

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